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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,792	01/15/2002	Hidetaka Natsume	NECW 19.349	6481

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/046,792	Applicant(s) NATSUME, HIDETAKA
	Examiner Joseph Nguyen	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *14-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kikushima et al (JP 10-163440).

Regarding claim 1, Kikushima et al discloses on figures 22-23 a semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors Q5, Q6 and a flip flop circuit containing a pair of driver transistors Q2, Q4 and a pair of load transistors Q1, Q3 wherein a first interconnection L1 formed from a first electrical conductor which is set on a semiconductor substrate 1, constitutes respective gate electrodes of said driver transistors, load transistors and transmission transistors; a second interconnection L2 including a second electrical conductor 15 which is formed within a first trench that is et in a first insulating film 11 lying on said semiconductor substrate, constitutes one of a pair of local interconnections cross coupling a pair of input/output terminals in said flip flop circuit; a third interconnection 18 which is formed on a second insulating film 17 lying on a region including the top surface of said second interconnection, constitutes the other one of said pair of local interconnections; and either said second interconnection or said

interconnection has a buried conductive section which is formed to fill up the inside of said trench, said second electrical conductor is disposed so as to come in contact with a drain region constituting a first driver transistor which is one of said pair of driver transistors; a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection, the gate electrode being in common to said first driver transistor; and a first interconnection which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors.

Regarding claim 2, Kikushima et al discloses on figures 22-23 said second interconnection 14 and said third interconnection 18 have an overlapping section separated by said second insulating film; and said second interconnection and said third interconnection together with said second insulating film lying there between constitute a capacitor element.

Regarding claim 3, Kikushima et al discloses on figures 22-23 said third interconnection is in contact with a contact section connected to said first interconnection; a contact section connected to a drain region of said second driver transistor; and a contact section connected to a drain region of said second load transistor.

Regarding claim 4, Kikushima et al discloses on figures 22-23 a semiconductor memory device having a SRAM in which a memory cell comprises a pair of transmission transistors Q5, Q6 and a flip flop circuit containing a pair of driver

transistors Q2, Q4 and a pair of load transistors Q1, Q3, wherein a first conductive film interconnection formed from a first conductive film which is set on a semiconductor substrate 1 constitutes respective gate electrodes of said driver transistors, load transistors and transmission transistors; an inlaid interconnection 15 set in a first insulating film 11 lying on said semiconductor substrate 1 constitutes one of a pair of local interconnections cross coupling a pair of input/output terminals in said flip flop circuit; and a second conductive film interconnection formed from a second conductive film which is set on a second insulating film lying on said first insulating film constitutes the other one of said pair of local interconnections, said inlaid interconnection being deposed so as to come in contact with a drain region constituting a first driver transistor which is one of said pair of driver transistors; a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode 6 formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor, and a first conductive film interconnection which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors.

Regarding claims 5-13, Kikushima et al discloses on figures 22-23 all the structures set forth in the claimed invention.

Response to Arguments

Applicant's arguments filed on 9/11/2003 have been fully considered but they are not persuasive.

Applicant argues that Kikushima et al. does not disclose the second electrical conductor formed within the first trench as now recited in claim 1. However, Kikushima et al. clearly discloses on figure 22 the second electrical conductor 15 formed within the first trench. Also, this second electrical conductor is in electrical contact with electrode 18 and source/drain region. As such, it functions as a local interconnect. In a similar manner, Kikushima et al. teaches that the inlaid interconnection 15 functions as a local interconnect as recited in claim 4 therein.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
November 20, 2003

GEORGE ECKERT
PRIMARY EXAMINER